VLSI Implementation of Turbo encoder and decoder for MIMO-OFDM systems using maximum a posteriori approach

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Abstract:

The demand for reliable and high-throughput communication systems has driven the development of advanced error-correction techniques like Turbo coding, which plays a crucial role in MIMO-OFDM systems. MIMO-OFDM systems are widely used in wireless standards, improving bandwidth efficiency by up to 40%, while reducing error rates in noisy environments by 60%. However, existing methods, such as Hamming codes, can only correct single-bit errors, making them inadequate for modern, high-data-rate communication systems.Hamming codes, while efficient for small-scale applications, struggle with burst errors and cannot provide the necessary error correction for complex communication systems like MIMO-OFDM. This project introduces a novel implementation of Turbo Encoder and Decoder using Recursive Systematic Codes (RSC) and the Maximum-a-Posteriori (MAP) algorithm. The Turbo Encoder improves data transmission reliability, while the Turbo Decoder using the MAP approach efficiently estimates transmitted bits, offering robust error correction. This VLSI-based design ensures enhanced performance and fault tolerance in high-data-rate MIMO-OFDM systems.***Keywords: Verilog HDL, Recursive Systematic Codes, Maximum-a-posteriori, Turbo Encoder and Decoder, MIMO-OFDM Systems, Communication, Error Correction Technique.***

1. INTRODUCTION

MIMO-OFDM Adopted Nano Communication Networks (MO-NCN) are essential tools in the realm of digital communication and data storage, ensuring the integrity and reliability of transmitted or stored information in the presence of errors. At its core, MO-NCN involves the addition of redundant bits to data, enabling the detection and correction of errors that may occur during transmission or storage processes. These codes are crucial in mitigating the effects of noise, interference, or hardware faults that can corrupt data. The concept of MO-NCN traces back to the early days of digital communication, where researchers recognized the need for mechanisms to detect and correct errors. Over time, various MO-NCN techniques have been developed, ranging from simple parity checks to more sophisticated algorithms capable of correcting multiple errors and detecting patterns of errors known as bursts.

MO-NCN operates on the principle of redundancy, where additional bits are added to the original data based on mathematical algorithms. These redundant bits enable the receiver to detect errors by comparing the received data with the expected data. In cases where errors are detected, MO-NCN algorithms use redundancy to correct the errors, restoring the original data to its intended state.

Finally, MO-NCN plays a fundamental role in ensuring the integrity of digital data, enabling robust communication and storage solutions in a wide range of applications, from wireless communication and satellite systems to computer memory and data centers. As digital technology continues to advance, MO-NCN techniques will remain indispensable for maintaining the integrity and reliability of digital information. Error correcting codes operate on the principle of adding redundancy to the original data such that errors can be detected and corrected at the receiver end. These codes typically add extra bits (parity bits or redundancy) to the original data based on mathematical algorithms.

MO-NCN algorithms are tailored to strike a delicate balance between hardware complexity, power consumption, and error correction efficiency. Engineers leverage specialized hardware architectures and optimization techniques to design MO-NCN circuits that meet the stringent requirements of modern digital systems. Moreover, MO-NCN modules must seamlessly integrate into larger communication or storage systems, adhering to established protocols and incorporating fault-tolerance mechanisms to handle errors within the MO-NCN circuitry itself.

MO-NCN is crucial for maintaining data reliability and integrity in various digital systems, including telecommunications, data storage, satellite communications, and computer memory. By employing MO-NCN, these systems can operate with higher accuracy and efficiency, even in the presence of adverse conditions that might introduce errors. As digital technology continues to advance, MO-NCN techniques will remain indispensable for ensuring the seamless and reliable operation of digital communication and storage systems.

2. LITERATURE SURVEY

Singh, S. Pratap, et al. [1] created Molecular Communication (MC), an interdisciplinary field of nano, bio, and communication technology. From biological to environmental to NBC defense, MC served practically every human need. However, MC lacked technical demonstration and progress. EEC improved MC system performance like any communication system. Recent publications showed VLSI implementations of C-RM and Hamming code.

Silva, Felipe, et al. [2] examined how microelectronics improved scalable and complicated circuit designs, increasing processing speed and storage capacity. In crucial radiation-exposed applications, reliability difficulties increased as electronic equipment scaled down, increasing defect rate. Transient effects from charged particles might impair memories. High MO-NCN use reduced data failures and improved memory reliability. The matrix region selection code (MRSC) was an MO-NCN that corrected nearby memory mistakes well but not nonadjacent errors. However, MRSC's 2-D structure made it difficult to implement in memory using one address at a time. The triple burst error correction based on region selection code (TBEC-RSC) translated MRSC into a 1-D structure.

Chu, Syuna-A Ke, et al. [3] suggested Guessing random additive noise decoding (GRAND) as a code-agnostic linear block code decoding method that tried to estimate the received word's error pattern to verify the codeword. GRANDAB limited test error patterns to implement a hard-detection decoder. This paper offered effective

strategies to decrease GRANDAB queries for systematic and cyclic codes. As the GRANAB corrected up to the code's error-correcting capabilities, these approaches used syndrome weight and cyclic codes to drastically reduce decoding time. The revolutionary hard-detection GRANDAB's VLSI design efficiently decoded up to 128 bits and corrected up to 3-bit mistakes at or above the code's error-correcting capabilities.

Kuo et al. [4] demonstrated the Consultative Committee for Space Data Systems (CCSDS) suggestion for short-block length Bose–Chaudhuri–Hocquenghem and binary low-density parity-check codes. Decoding nonbinary low-density parity-check (NB-TE-MO-NCN) codes was too difficult, despite their error-correction capabilities. Our study examined whether a RISC-V soft-core processor and vector coprocessor might implement NB-TE-MO-NCN coding for space telecommand link applications. This research aimed to remove the need for separate decoder hardware, allowing the tailored general-purpose CPU to do other important onboard functions.

Christoph Pichler, et al. [5]. Quantum MO-NCN might find and fix these mistakes. However, much quantum error correction research was theoretical or restricted to hardware models. Development and assessment of comparable codes sometimes involved painstaking trial-and-error procedures. They proposed an open-source platform to let engineers and researchers automatically apply MO-NCN for a specific application and an automated noise-aware quantum circuit simulation. This technique dramatically improved MO-NCN development and assessment, according to case studies.

Wu, Yujun, Bin Wu, et al. [6] created the QC-TE-MO-NCN code, which supports hardware and has good error correction. Wi-Fi 6 selected it as a channel encoding technique. Sending user input with integer symbols and perfect rate matching required shortening, puncturing, or repeating procedures. The receiver faced more than 106 circumstances due to user data size uncertainty, modulation selectivity, and spatial stream differences. Other computationally demanding operations used up the receiver's time slot allotment. Typical were demodulation and decoding. The receiver has to swiftly reverse demodulated data. This literature introduced a co-processing approach and VLSI architecture for all code lengths, rates, and processing parameters.

Pokhrel, Nabin Kumar, et al. [7] introduced integer codes that rectify burst asymmetric faults. Electronic networks and VLSI memory might employ the computer-generated codes. The literature examined the likelihood of erroneous decoding for various bit error rates to assess the suggested codes. The codes were also rate-efficiently examined. Results indicated they needed fewer check-bits than ideal burst error correcting codes for various data lengths.

Saini, Madan Lal, et al. [8] performed various single- and double-bit error correcting and detecting codes were available. The efficiency of an error correcting code was evaluated by its error correction capabilities and redundancy. This paper presented new single bit and double bit error correcting codes which had lower redundancy compared to other existing codes. In this literature, the number of parity bits over the message bits for Hamming, BCH, RS Code, and DEC were examined and overhead was calculated.

Ponmalar, VJ Beulah Sherin, et al. [9] conceived and implemented low-density parity check in VLSI designs. A digital communication system usually has problems owing to noise, distortion, and interference during data transfer and different methods employed to fix them. A third-generation wireless system transmitted speech and control messages using convolutional coding. The current system employed turbo codes and the belief propagation algorithm to construct VLSI with low bit error rate and signal-to-noise ratio but high decoding error rate and complexity.

Boncalo, Oana, et al. [10] introduced Gradient Descent Symbol Update, an iterative decoding approach for real number parity-based MO-NCN, and its hardware design. The decoding procedure used gradient descent optimization and binary maximum likelihood error correction. We showed the gradient descent symbol update convergence rate and error correction performance for a parity-based BCH (26,16) code. Also shown were FPGA implementation results for the decoder architecture.

3. PROPOSED METHODOLOGY

This phase offers an in-depth analysis of the proposed MIMO-OFDM programs which might be the focus of the MAP-TED system, which has been delivered. Within the context of information transmission, MAP-TED operates in a manner that is each methodical and complex to guarantee dependable errors correction. To generate encoded records immune to mistakes, the MAP-TED encoder entails the use of Recursive Systematic Convolutional (RSC) encoders on the side of interleaving. To simulate the situations that exist inside actual time, this statistic is sent through a loud channel in a simulated transmission. The technique of interpreting includes the information which has been encoded being divided into segments and then fed into RSC-MAP decoders. These decoders are characteristic in an iterative way, making use of interleaving and engaging in records exchange to enhance mistakes correction. Despite mistakes that were delivered sooner or later of transmission, the goal is to correctly reconstruct the records that turn out to be to start with transmitted.

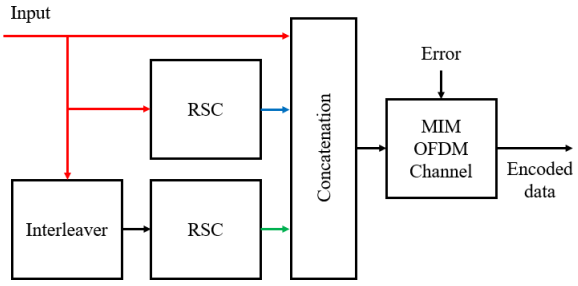

Figure 1: Proposed MAP-TED encoder block diagram.

MAP-TED encoder

The block diagram of the proposed MAP-TED encoder, which makes use of an RSC encoder with direct input. The method begins with the records that is input, that is then considered with the aid of the RSC1 encoder. A technique of interleaving is performed at the output of RSC1 before it's far sent via the RSC2 encoder. Data that has been encoded is created by way of concatenating the outputs of RSC1 and RSC2 which have been produced as a result, at the side of the preliminary enter. An error-correcting code known as the RSC encoder is a type of code that encodes enter bits in a methodical way even as simultaneously incorporating feedback from bits that have been encoded inside the past.

The interleaving step provides a further layer of complexity to the encoding system, which is already complicated by way of the reality that there are RSC encoders (RSC1 and RSC2) working together in coordination. The bits are rearranged thru the system of interleaving to lessen the effect of burst mistakes that occur during transmission. Following that, the encoded statistics is despatched thru the MIMO-OFDM channel for transmission. The representation of this channel considers the existence of errors, more specifically Additive White Gaussian Noise (AWGN).

MAP-TED decoder

Figure 2 depicts the interpreting technique this is applied inside the MAP-TED decoder this is being proposed. Data that has been encoded is divided into three streams: the first circulation incorporates the encoded data that became at first encoded, the second one flow consists of facts from RSC1, and the 1/3 circulation contains records from RSC2. This record is then sent to two RSC-MAP decoders for processing. Both the authentic encoded statistics and the facts from RSC1 are processed with the aid of Decoder 1, while Decoder 2 processes the interleaved encoded statistics as well as the facts from RSC2.

Iterative surroundings are brought between Decoder 1 and Decoder 2, with interleavers and deinterleavers performing the facilitation of this environment. It is possible for the 2 decoders to proportion data with each other via this iterative technique, which results in an improvement in the errors-correction skills. The steps of interleaving and deinterleaving are extremely crucial in this manner due to the fact they permit the decoders to take benefit of the advantages of diversity and make it less complicated for them to correct a variety of errors. Finally, the output of Decoder 1 represents the decoded records, which, in a super global, must be same to the statistics that became to start with enter without any mistakes. This demonstrates that the MAP-TED decoding scheme that was proposed is effective.

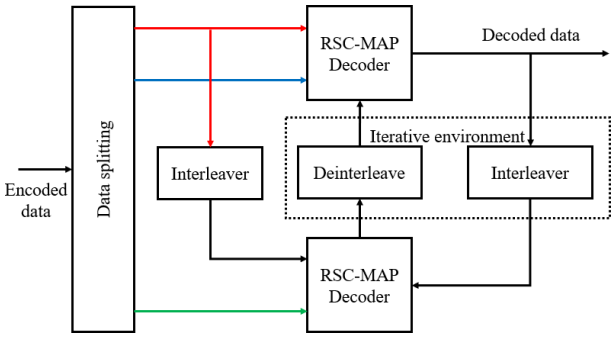

Figure 2: Proposed MAP-TED decoder block diagram.

4. EXPERIMENTAL ANALYSIS

In this section, a comprehensive simulation analysis of the MAP-TED system that has been proposed is presented. Simulations are carried out in this location with the assistance of the Xilinx-Vivado software tool. The result of the simulation is depicted in **Figure 3**, which includes the clk and rst as primary inputs, data_in as an 8-bit data input, and enc_out as a 32-bit MAP-TED encoded output, which includes errors. Lastly, the output of the MAP-TED decoder is the output that is free of errors.

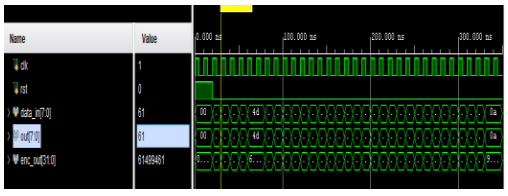

Figure 3: Simulation output

The utilization of resources for the proposed MAP-TED implementation is illustrated in **Figure 4**, which provides insights into the matter. "LUTs" is an abbreviation that stands for "Look-Up Tables," which are essential elements that are found in digital circuits. Since only 16 of the 78,600 available LUTs are utilized in this scenario, it can be concluded that the design is relatively simple in terms of the amount of logic that is involved. Input/Output Blocks, also known as IoBs, play a role in connecting the design to external devices. The utilization of 49 out of 250 IoBs indicates that these resources are utilized in a moderate manner. To maximize the effectiveness of the design and make the most of the resources that are at one's disposal, it is essential to visualize the utilization of the available space.

Resource	Utilization	Available	Utilization...
LUT	16	78600	0.02
IO	49	250	19.60

Figure 4: Design summary.

In the realm of digital design, setup time is an essential metric that denotes the minimum amount of time that must pass before a signal is able to become stable before the subsequent clock edge.

In Figure 5, the total delay of 7.436 nanoseconds is broken down into its component parts: logic delays, which account for 3.5 nanoseconds, and net delays, which account for 3.9 nanoseconds. This information is essential for ensuring that signals are stable and valid at the input of the flip-flops, as well as for meeting timing requirements and avoiding violations of setup time.

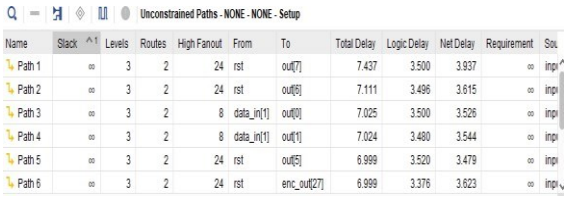

Figure 5: Setup Time summary.

Figure 6 provides a concise summary of hold time, which refers to the minimum amount of time that a signal must be held stable after the clock edge. There is a total delay of 2.064 nanoseconds, making up 1.328 nanoseconds of logic delay and 0.736 nanoseconds of net delay. Effective management of hold times is absolutely necessary in order to avoid the corruption of data and to keep the signals' integrity intact while the clocking process is being carried out.

Figure 6: Hold Time summary.

Figure 7 provides a comprehensive overview of the power utilization that is included in the MAP-TED design that is being proposed. Within the context of power consumption, both dynamic and static components are broken down in detail. There are contributions from signals, logic, and I/O Blocks that are further broken down into the dynamic power, which is 14.852uW altogether. The amount of power that is lost out of the circuit when it is in a static state is 0.226 uW, which is referred to as static power. The total power utilization of 15.1 uW offers a comprehensive understanding of the power requirements, which is helpful in optimizing power consumption and taking efficiency into consideration during the design process. Applications in which power consumption is a primary concern, such as those involving energy-efficient systems or devices powered by batteries, require this information to function properly.

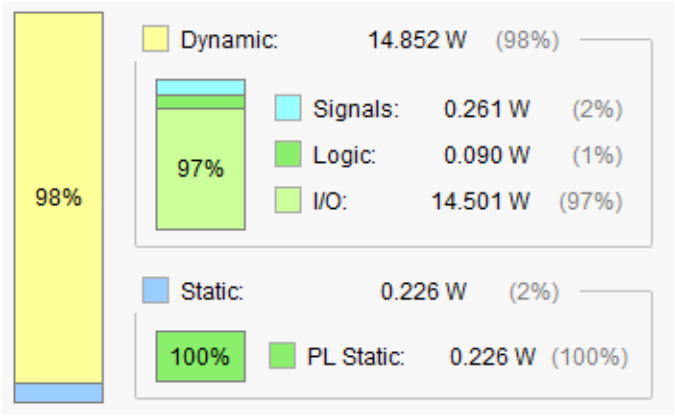

Figure 7: Power summary

It is clear from looking at Table 1 that the proposed system demonstrates a significant improvement in terms of resource utilization when compared to the system that is currently in place. According to the number of LUTs, the proposed system makes use of sixteen LUTs, whereas the current system makes use of thirty-five LUTs. Consequently, this represents a significant decrease of 54.3%. To a similar extent, the proposed system makes use of 49 IoBs, whereas the system that is currently in place makes use of 76 IoBs. The improvement in this case amounts to a significant reduction of 35.5% in the amount of IoB usage. These reductions are illustrative of the effectiveness and optimization that the proposed system has achieved in terms of making better use of the resources provided by the hardware.

Resource	Existing System	Proposed System
LUTs	35	16
IoBs	76	49

Table 1: Area performance comparison.

The system that is being proposed demonstrates significant improvements in delay measurements in comparison to the system that is currently in place. As can be seen in Table 2, the proposed system, in terms of setup delay, demonstrates reductions in both the logic setup delay and the net setup delay, with improvements of 31.7% and 16.7%, respectively. When compared to the system that is currently in place, the proposed system can achieve a total setup delay reduction of 24.3%. When it comes to hold delays, the proposed system demonstrates significant reductions in both logic and net hold delays, with improvements of 51.8% and 49.3%, respectively, in the latter category. When compared to the current system, the proposed system has a significant improvement of 34.5% in terms of the total delay; this improvement is significant. The proposed design has the potential to achieve higher levels of efficiency and faster processing speeds, as indicated by these reductions.

Table 2: Delay performance comparison.

Dealy (ns)	Existing System	Proposed System
Logic Setup Delay	5.13	3.5
Net Setup Delay	4.69	3.9
Total Setup Delay	9.8	7.436
Logic Hold Delay	2.72	1.328
Net Hold Delay	1.451	0.736
Total Hold Delay	4.10	2.064
Total Delay	13.9	9.1

As can be seen in Table 3, the proposed system demonstrates significant improvements in power performance in comparison to the system that is currently in place. The proposed system exhibits reductions in signal power, logic power, and IoB power, with the latter three exhibiting improvements of 45.8%, 44.4%, and 13.7%, respectively. In comparison to the system that is currently in place, the proposed system brings about a 14.4% reduction in the total dynamic power consumption. Furthermore, the proposed system demonstrates a reduction of 40.5% in the amount of static power observed. The total amount of power that is consumed by the proposed system is significantly lower than the amount that is consumed by the system that is currently in place by 15.0%.

These reductions correspond to a more effective utilization of power and could potentially result in lower energy requirements for the design that is being proposed.

Power (uw)	Existing Filter	Proposed Filter
Signal Power	0.481	0.261
Logic Power	0.162	0.090
IoB Power	16.81	14.501
Total Dynamic Power	17.4	14.852
Static Power	0.38	0.226
Total Power Consumption	17.78	15.1

Table 3: Power performance comparison.

5. CONCLUSION

To ensure the transmission of data in a reliable manner even when channel-induced errors are present, the MAP-TED that has been proposed incorporates a sophisticated error-correction mechanism. The encoder uses RSC encoders that incorporate interleaving to encode the input statistics before its transmission thru a MIMO-OFDM channel with simulated transmission mistakes. When it comes to decoding, the MAP-TED decoder makes use of RSC-MAP decoders, each of that is chargeable for handling a different element of the encoded data.

The mistakes-correction capabilities are advanced via the iterative technique that occurs between those decoders. This process is made viable with the resource of interleavers and deinterleavers, which ensures that the unique facts is recovered in a reliable and correct manner. The MAP-TED system is designed to offer a dependable solution for conversation systems which may be running in hard environments. This is accomplished using a scientific encoding and iterative deciphering method, which targets to reduce mistakes which may be added throughout transmission itself.

A comprehensive approach to blunders correction is confirmed by using the tool that has been proposed. This technique combines the advantages of recursive encoding, interleaving, and iterative deciphering on the way to attain excessive fidelity in all components of information recuperation.

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